Notice of Allowability	Application No.	Applicant(s)	
	09/395,294	WILSON, SOPHIE	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Appeal Brief filed 9/6/06*.

2. ☒ The allowed claim(s) is/are *17, 18, 19, 20, 22, 24, 27, 28, 31, 32 and 33*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/20/2006

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. According to MPEP 606.01, the title has been changed to read:

   a. "Identification Bit at a Predetermined Instruction Location that Indicates Whether the Instruction is One or Two Independent Operations and Indicates the Nature of the Operations Executing in Two Processing Channels"

3. Authorization for this examiner's amendment was given in a telephone interview with Bryan Wade on November 16, 2006.

   a. The claims have been amended according to the attached document entitled "U.S. Patent Application No. 09/395,294 - Proposed Claim Amendments" (5 pages in total) informally submitted by Applicant to Examiner.

4. The following is an examiner's statement of **reasons for allowance**:

   a. Referring to claim 17, the prior art of record has not taught or suggested "wherein the decode unit is operable to identify certain combinations of the two independent operations based on the at least one identification bit" in combination with the claimed decode unit, the first and second processing channels, and the two other claimed wherein clauses.

b. Referring to claim 24, the prior art of record has not taught or suggested "wherein determining whether the instruction defines the single operation or two independent operation includes determining whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines two independent operations" in combination with the claimed decoding, supplying, controlling and determining steps.

c. Referring to claim 28, the prior art of record has not taught or suggested "wherein the at least one identification bit indicates the nature of the two independent operations when the instruction defines the two independent operations" in combination with the claimed process, supply and control steps.

d. Referring to claim 32, the prior art of record has not taught or suggested "reading the at least one identification bit of each instruction to determine when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation" in combination with the claimed fetching, decoding and supplying steps steps.

e. Referring to claim 33, the prior art of record has not taught or suggested "to decode an instruction of the VLIW received during an instruction fetch to determine when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation, based on the

at least one identification bit of the instruction" in combination with the claimed process, supplying and simultaneously execute steps.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

tlm

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11/20/2006

U.S. Patent Application No. 09/395,294 - Proposed Claim Amendments

17. (*Currently Amended*) A system to process very long instruction words (VLIWs), the system comprising:

a decode unit to decode an instruction of a VLIW received during an instruction fetch, wherein all instructions of the VLIW have the same predetermined instruction bit length; and

first and second processing channels, each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit and at least one other of the functional units of each processing channel being a memory access unit;

wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction and to control the first and second processing channels based on the determination[[.]];

wherein the decode unit is operable to identify certain combinations of the two independent operations based on the at least one identification bit; and

wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation, and a fourth combination denotes a long instruction.

18. (*Previously Presented*) The system according to claim 17, wherein, when the decode unit determines that the instruction defines two independent operations, the decode unit is operable to control the first channel to implement one of the two independent operations and the second channel to implement the other of the two independent operations, and wherein the first and second channels execute their respective independent operations simultaneously.

19. (*Previously Presented*) The system according to claim 17, wherein, when the decode unit determines that the instruction defines a single operation, the decode unit is operable to control the first and second processing channels to cooperate to execute the single operation.

20. (*Previously Presented*) The system according to claim 17, wherein the first and second processing channels share at least one common register file and are capable of simultaneously accessing the at least one common register file.

21. (*Canceled*)

22. (*Currently Amended*) The system according to claim [[21]] 17, wherein the instruction has a length of n bits, and the at least one predetermined bit location includes the n/2th bit and the nth bit.

23. (*Canceled*)

24. (*Currently Amended*) A method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length, the method comprising:

decoding an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations;

when the instruction defines two independent operations, supplying one of the independent operations to a first processing channel having a first plurality of functional units including a first data processing unit and a first memory access unit, and supplying the other of the independent operations to a second processing channel having a second plurality of functional units including a second data processing unit and a second memory access unit, wherein the two independent operations are executed simultaneously; and

when the instruction defines a single operation, controlling the first and second processing channels to cooperate to execute the single operation[[.]];

wherein decoding the instruction includes determining whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction; and

wherein determining whether the instruction defines the single operation or the two independent operations includes determining whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations.

25. (*Canceled*)

26. (*Canceled*)

27. (*Currently Amended*) The method according to claim [[25]] 24, wherein determining whether the instruction defines the single operation or the two independent operations is based on an n/2th bit and an nth bit of the instruction having n bits.

28. (*Currently Amended*) An article comprising a medium for storing commands to enable a processor-based system to:

process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length, wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction;

when the instruction defines two independent operations, supply one of the independent operations to a first processing channel and supply the other of the independent operations to a second processing channel, wherein the two independent operations are executed simultaneously, and wherein the at least one identification bit indicates the nature of the two independent operations when the instruction defines the two independent operations; and

when the instruction defines a single operation, control the first and second processing channels to cooperate to execute the single operation.

29. (*Canceled*)

30. (*Canceled*)

31. (*Currently Amended*) The article according to claim [[29]] 28, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on an n/2th bit and an nth bit of the instruction having n bits.

32. (*Currently Amended*) A method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, the method comprising:

fetching the VLIW from a program memory;

decoding each instruction of the VLIW, wherein decoding each instruction includes reading the at least one identification bit of each instruction to determine:

a) whether the instruction defines a single operation or two independent operations, and

b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation[[.]]; and

when the instruction defines two independent operations, supplying one of the independent operations to a first processing channel having a first plurality of functional units including a first data processing unit and a first memory access unit, and supplying the other of the independent operations to a second processing channel having a second plurality of functional units including a second data processing unit and a second memory access unit, wherein the two independent operations are executed simultaneously.

33. (*Currently Amended*) An article comprising a medium for storing commands to enable a processor-based system to:

process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine:

a) whether the instruction defines a single operation or two independent operations based on the at least one identification bit of the instruction, and

b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation, based on the at least one identification bit of the instruction[[.]]; and

when the instruction defines two independent operations,

a) supply one of the independent operations to a first processing channel having a first plurality of functional units including a first data processing unit and a first memory access unit,

b) supply the other of the independent operations to a second processing channel having a second plurality of functional units including a second data processing unit and a second memory access unit, and

c) simultaneously execute the two independent operations.